Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-162 (Cancelled)

163. (Currently Amended) A chip package comprising:

a die-surrounding layer;

a die between a first portion of said die-surrounding layer and a second portion of said die-surrounding layer, wherein said die has a top surface substantially coplanar with a top surface of said die-surrounding layer, wherein said die comprises a metal pad at a top side of said die;

a first dielectric layer on said top surface of said die and said top surface of said die-surrounding layer;

a patterned metal layer over said first dielectric layer, said top surface of said die and said top surface of said die-surrounding layer, wherein said patterned metal layer is connected to said metal pad of said die through an opening in said first dielectric layer, wherein said patterned metal layer comprises a portion of a comb-shaped capacitor; and;

~~a comb-shaped capacitor over said first dielectric layer; and~~

a second dielectric layer on said patterned metal layer ~~and said comb-shaped capacitor,~~ and over said first dielectric layer, said top surface of said die and said top surface of said die-surrounding layer.

164. (Currently amended) The chip package in claim 163, wherein said portion of said comb-shaped capacitor is ~~comprises a portion~~ vertically over said first portion of said die-surrounding layer.

165. (Cancelled)

166. (Previously Presented) The chip package in claim 163, wherein said first dielectric layer comprises polyimide.

167. (Previously Presented) The chip package in claim 163, wherein said first dielectric layer comprises benzocyclobutene (BCB).

168. (Previously Presented) The chip package in claim 163, wherein said patterned metal layer comprises electroplated copper.

169. (Previously Presented) The chip package in claim 163, wherein said second dielectric layer comprises polyimide.

170. (Previously Presented) The chip package in claim 163, wherein said second dielectric layer comprises benzocyclobutene (BCB).

171. (Currently amended) The chip package in claim 163 further comprising multiple solder bumps, configured for external connection, vertically over said top surface of said die-surrounding layer.

172. (Cancelled)

173. (Currently amended) The chip package in claim 163 further comprising multiple gold bumps, configured for external connection, vertically over said top surface of said die-surrounding layer.

174-175. (Cancelled)

176. (Currently amended) The chip package in claim 163 further comprising a substrate under said die and ~~under~~ said first and second portions of said die-surrounding layer.

177. (Previously Presented) The chip package in claim 176, wherein said substrate comprises a silicon substrate.

178. (Previously Presented) The chip package in claim 163, wherein said die-surrounding layer comprises epoxy.

179. (Currently amended) A chip package comprising:

a die-surrounding layer;

a die between a first portion of said die-surrounding layer and a second portion of said die-surrounding layer, wherein said die has a top surface substantially coplanar with a top surface of said die-surrounding layer, wherein said die comprises a first metal pad at a top side of said die and a second metal pad at said top side;

a first dielectric layer on said top surface of said die and on said top surface of said die-surrounding layer; and

a patterned metal layer over said first dielectric layer, said top surface of said die and said top surface of said die-surrounding layer, wherein said patterned metal layer is connected to [[a]] said first metal pad of said die through a first opening in said first dielectric layer, and wherein said patterned metal layer is connected to [[a]] said second metal pad of said die through a second opening in said first dielectric layer, wherein said first metal pad is connected to said second metal pad through said patterned metal layer, wherein said patterned metal layer comprises a portion of a passive device.; and

~~a passive device over said first dielectric layer.~~

180. (Currently Amended) The chip package in claim 179, wherein said die-surrounding layer comprises ~~an~~ epoxy.

181. (Currently Amended) The chip package in claim 179 further comprising multiple solder bumps, configured for external connection, vertically over said top surface of said die-surrounding layer.

182. (Previously Presented) The chip package in claim 179, wherein said first dielectric layer comprises polyimide.

183. (Previously Presented) The chip package in claim 179, wherein said first dielectric layer comprises benzocyclobutene (BCB).

184. (Currently amended) The chip package in claim 179 further comprising a second dielectric layer on said patterned metal layer ~~and said passive device,~~ and over said first dielectric layer, said top surface of said die and said top surface of said die-surrounding layer.

185. (Previously Presented) The chip package in claim 184, wherein said second dielectric layer comprises polyimide.

186. (Previously Presented) The chip package in claim 184, wherein said second dielectric layer comprises benzocyclobutene (BCB).

187. (Previously Presented) The chip package in claim 179, wherein said patterned metal layer comprises a ground bus connecting said first metal pad to said second metal pad.

188. (Previously Presented) The chip package in claim 179, wherein said patterned metal layer comprises a power bus connecting said first metal pad to said second metal pad.

189. (Previously Presented) The chip package in claim 179, wherein said patterned metal layer comprises a signal trace connecting said first metal pad to said second metal pad.

190. (Currently Amended) The chip package in claim 179, wherein said passive device comprises a filter, ~~over said first dielectric layer.~~

191. (Currently Amended) The chip package in claim 179, wherein said passive device comprises an inductor, ~~over said first dielectric layer.~~

192. (Currently Amended) The chip package in claim 179, wherein said passive device comprises a capacitor, ~~over said first dielectric layer.~~

193. (Currently Amended) The chip package in claim 179, wherein said passive device comprises a resistor. ~~over said first dielectric layer.~~

194. (Currently Amended) The chip package in claim 179 further comprising a substrate under said die and ~~under~~ said first and second portions of said die-surrounding layer.

195. (Currently Amended) The chip package in claim 194, wherein said substrate comprises a silicon substrate.

196. (Currently Amended) The chip package in claim 179, wherein said portion of said passive device ~~comprises a portion~~ is vertically over said first portion of said die-surrounding layer.

197. (Currently Amended) A chip package comprising:

a die-surrounding layer;

a die between a first portion of said die-surrounding layer and a second portion of said die-surrounding layer, wherein said die has a top surface substantially coplanar with a top surface of said die-surrounding layer, wherein said die comprises a first metal pad at a top side of said die and a second metal pad at said top side;

a first dielectric layer on said top surface of said die and on said top surface of said die-surrounding layer; and

a patterned metal layer over said first dielectric layer, said top surface of said die and said top surface of said die-surrounding layer, wherein said patterned metal layer comprises a ground piece connected to ~~a~~ said first metal pad of said die through a first opening in said first dielectric layer, and connected to ~~a~~ said second metal pad of said die through a second opening in said first dielectric layer, wherein said first metal pad is connected to said second metal pad through said ground piece, wherein said patterned metal layer comprises a portion of a passive device.; ~~and~~

~~a passive device over said first dielectric layer.~~

198. (Currently Amended) The chip package in claim 197, wherein said passive device comprises an inductor, ~~over said first dielectric layer.~~

199. (Currently Amended) The chip package in claim 197, wherein said passive device comprises a resistor, ~~over said first dielectric layer.~~

200. (Previously Presented) The chip package in claim 197, wherein said die-surrounding layer comprises epoxy.

201. (Currently Amended) The chip package in claim 197, wherein said passive device comprises a capacitor, ~~over said first dielectric layer.~~

202. (Previously Presented) The chip package in claim 197, wherein said first dielectric layer comprises polyimide.

203. (Currently Amended) The chip package in claim 197 further comprising a second dielectric layer on said patterned metal layer, ~~and on said passive device.~~

204. (Previously Presented) The chip package in claim 197, wherein said first dielectric layer comprises benzocyclobutene (BCB).

205. (Currently Amended) The chip package in claim 197 further comprising multiple solder bumps, configured for external connection, vertically over said top surface of said die-surrounding layer.

206. (Currently Amended) The chip package in claim 197 further comprising a substrate under said die and ~~under~~ said first and second portions of said die-surrounding layer.

207. (Previously Presented) The chip package in claim 206, wherein said substrate comprises a silicon substrate.

208. (Currently Amended) The chip package in claim 197, wherein said passive device comprises a filter. ~~over said first dielectric layer.~~

209. (Previously Presented) The chip package in claim 197, wherein said patterned metal layer comprises electroplated copper.

210. (Previously Presented) The chip package in claim 179, wherein said patterned metal layer comprises electroplated copper.